REMARKS

Claims 6-9 and 11-19 are pending in the present application. Replacement claims 6, 11 and 16 have been presented herewith.

Objection to Amendment

The Amendment filed October 31, 2002, has been objected to under 35 U.S.C. 132 as allegedly introducing new matter into the disclosure. The Examiner has asserted that the amended material "the contact hole 52 and wiring 54 connect to the gate" must be canceled.

Although Applicant does not necessarily concede that the above noted material constitutes new matter, the paragraph beginning on page 13, line 12 of the specification has been amended to delete reference to previously presented proposed Fig. 1(i), which has been cancelled. Accordingly, the Examiner is respectfully requested to withdraw the objection to the Amendment under 35 U.S.C. 132, for at least the above reasons.

Drawings

The proposed drawing correction as filed on October 31, 2002, has been disapproved under 37 C.F.R. 1.121(a)(6), as allegedly introducing new matter into the drawings. The Examiner has asserted that the original disclosure does not support the showing of "the contact holes 52 and the connecting wire 54 are directly on the gate".

Although Applicant does not necessarily concede that the above noted material constitutes new matter, previously submitted Fig. 1(i) has been canceled. Accordingly, the Examiner is respectfully requested to withdraw this objection to the drawings.

The drawings have also been objected to under 37 C.F.R. 1.83(a), as failing to show every feature of the invention specified in the claims. The Examiner has required that the insulating layer, the contact hole and the connecting wire be shown, or that these features be canceled from the claims. This objection, insofar as it may be applicable with respect to the application in view of this Amendment, is respectfully traversed for the following reasons.

Independent claims 6, 11 and 16 have each been respectively amended to feature "an insulating layer, a contact hole and a connecting wire formed above a surface of the substrate".

As described on page 13 of the original specification, after side-wall 37 is formed by anisotropic etching as shown in Fig. 1(h), an insulating layer, a contact hole and aluminum wiring is conducted by a normal process, to thus complete the MOSFET. Clearly, these features including the insulating layer, the contact hole and the connecting wire are formed above a surface of substrate 31 as illustrated in Fig. 1(h), and clearly are features that are necessary to complete manufacture of the semiconductor device. The provision of these features as above the substrate is apparent, and is clearly supported and described on page 13 of the original specification, as noted above.

Applicant respectfully submits that claims 6, 11 and 16 as amended should be considered in compliance with 35 U.S.C. 132, because page 13 of the original specification clearly supports forming an insulating layer, a contact hole and aluminum wiring above the surface of the substrate.

From the standpoint of 37 C.F.R. 1.83(a), Applicant respectfully submits that the insulating layer, the contact hole and the aluminum wiring as above the surface of the substrate is claimed in a broad sense, and that these features should be considered in a general sense as inherent in Fig. 1(h) of the application. In other words, one of ordinary skill would readily understand that these features are generally above the surface of substrate 31 of Fig. 1(h), and inherent as part of the completed MOSFETS.

Accordingly, Applicant respectfully submits that the drawings should be considered as in compliance with 37 C.F.R. 1.83(a). **If this particular objection to the drawings is to be maintained, any comments offered by the Examiner regarding proposed corrections to Fig. 1(h) that would be acceptable to show the insulating layer, the contact hole and the aluminum wiring as supported on page 13 of the original specification, would be greatly appreciated.**

Claim Rejections-35 U.S.C. 102

Claims 6-9 and 11-19 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Yoo et al. reference (U.S. Patent No. 5,605,853). This rejection is respectfully traversed for the following reasons.

As emphasized in the Remarks section of the Amendment dated October 31, 2002, floating gate 21 in Figs. 2-7 of the Yoo et al. reference cannot be formed directly on field oxide (FOX) layer 12, and thus cannot be interpreted as the protective layer of claim 6 for example. Particularly, layer 21 of the Yoo et al. reference is merely described as a floating gate **over** FOX layer 12 (see column 3, lines 15-17).

It should be understood that to function, a floating gate in theory must necessarily exchange charges with a diffusion layer formed in the surface of a semiconductor substrate. Thus, the floating gate must typically be formed on a relatively thin insulating layer, such as a tunnel oxide layer, so that exchange of charges between the diffusion layer and the floating gate may occur. Floating gates generally are not formed on a FOX layer, because exchange of charges between the floating gate and a corresponding semiconductor substrate through the relatively thick FOX layer would not occur.

In order to emphasize this point, enclosed as of interest is an I.E.E.E. Electron Device Letters publication by Haddad et al., specifically concerning flash memory cells. As described in the first column on page 117 of the publication, the gate oxide used is less than 120Å thick and the erasure mechanism is dominated by Fowler-Nordheim (F-N) tunneling. Accordingly, it should thus be understood by one of ordinary skill that in order to perform writing and deletion by means of F-N tunneling in flash memory cells, it is necessary to use a gate oxide having a thickness of approximately 120Å. Particularly, if the gate oxide is too thick, it is impossible to inject and emit electrons

through the gate oxide into the floating gate by means of F-N tunneling.

The Mizutani reference (U.S. Patent No. 4,637,128) is also enclosed as of interest, in an effort to further emphasize this point. As described beginning in column 4, line 57 of the Mizutani reference, after the ion implantation step, a field insulation layer 60 having a thickness of 6000Å is formed, as shown in Fig. 4D. In contrast, as described in column 5, lines 14-18 of the Mizutani reference, a thermal oxide film 66 is formed to be so thin so as to be generally removed in the patterning step of the poly-Si layer, but is not removed at the portion below the floating gate electrode 68. That is, a relatively thin oxide layer is formed under the floating gate, as opposed to the relatively thicker field oxide layer. Thus, it should be understood that floating gate electrodes in general are formed on relatively thin gate oxides, as opposed to relatively thick field oxide layers.

The Examiner has asserted in the Response to Arguments section on page 7 of the Final Office Action dated January 10, 2003, that one of ordinary skill should conclude "without any reasonable doubt" that layer 21 of the Yoo et al. reference is formed on FOX layer 12. However, as emphasized previously and as evidenced by the enclosed references submitted as of interest, functional floating gates are typically formed on relatively thin gate oxides of approximately 120Å, not relatively thick field oxides. Contrary to the Examiner's assertion, Applicant respectfully submits that one of ordinary skill would thus understand that floating gate 21 in Figs. 2-7 of the Yoo et al. reference cannot be formed on FOX layer 12 and be a functional floating gate. It

consequently follows that it cannot be concluded "without any reasonable doubt" that layer 21 of the Yoo et al. reference is formed on FOX layer 12, as asserted by the Examiner. Again, it is emphasized that floating gate 21 of the Yoo et al. reference is merely described as formed **over** FOX layer 12.

Accordingly, Applicant respectfully submits that because floating gate 21 of the Yoo et al. reference cannot be formed on FOX layer 12 and thus cannot be interpreted as the protective layer of the claims, the semiconductor devices of respective independent claims 6, 11 and 16 distinguish over the Yoo et al. reference as relied upon by the Examiner. This rejection of claims 6-9 and 11-19 is therefore improper for at least these reasons, in addition to the reasons as set forth in the Amendment dated October 31, 2002.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding objections and rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

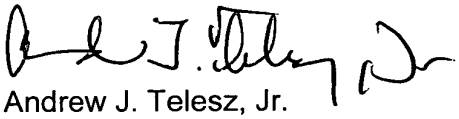
Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to May 10, 2003 for the period in which to

file a response to the outstanding Final Office Action. The required fee of $110.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

AJT:dmc

VOLENTINE FRANCOS, P.L.L.C.
12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Enclosures: Version with Marked-Up Changes
Copy of Mizutani Patent
Copy of IEEE Publication

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Specification:

Page 13, lines 12-17:

Thereafter, the side-wall 37 is formed by implementing the anisotropic etching such as the RIE with respect to the oxide layer 36 (FIG. 1(h)). Then, the insulating layer [~~50~~] and the contact [~~holes~~ 52] hole are formed, and the aluminum wiring [~~54~~] is conducted by the normal processes, thus completing the MOSFET [(FIG. 1(i))].

Additions/Deletions to the Claims:

6. (Four Times Amended) A semiconductor device comprising:

first and second gates formed on active regions of a substrate, said first and second gates each consisting of a refractory metal layer on a polysilicon layer;

a field oxide formed on the substrate between said first and second gates;

side walls formed on side surfaces of said first and second gates, said side walls being a silicon oxide film;

a protective layer formed selectively on said field oxide to prevent overetching of said field oxide, said protective layer being a material different than said field oxide; and

an insulating layer [formed on the substrate, said first and second gates, said side walls, said field oxide and said protective layer;], a contact [holes] hole [formed through said insulating layer;], and a connecting wire [coupled to said first and second gates through said contact holes] formed above a surface of the substrate.

11. (Twice Amended) A semiconductor device comprising:

a gate formed on an active region of a substrate;

a field oxide formed on the substrate adjacent the active region;

a protective layer formed on said field oxide to prevent overetching of said field oxide, said protective layer being a material different than said field oxide; and

an insulating layer [formed on the substrate including said gate, said field oxide and said protective layer;], a contact hole [formed through said insulating layer;], and a connecting wire [coupled to said gate through said contact hole] formed above a surface of the substrate,

said protective layer being formed on said field oxide only.

16. (Twice Amended) A semiconductor device comprising:

a gate formed on an active region of a substrate, said gate consisting of a refractory metal layer on a polysilicon layer;

side walls formed on side surfaces of said gate, said side walls being a silicon oxide film;

a field oxide formed on the substrate adjacent the active region;

a protective layer formed on said field oxide to prevent overetching of said field oxide, said protective layer being a material different than said field oxide; and

an insulating layer [formed on the substrate, said gate, said side walls, said field oxide and said protective layer;], a contact hole [formed through said insulating layer;], and a connecting wire [coupled to said gate through said contact hole] formed above a

surface of the substrate,

said protective layer being formed on said field oxide only.

IEEE ELECTRON DEVICE LETTERS, VOL. 10, NO. 3, MARCH 1989

Degradations Due to Hole Trapping in Flash Memory Cells

SAMEER HADDAD, CHI CHANG, BALAJI SWAMINATHAN, AND JIH LIEN

Abstract—Degradation in the hot-electron programmability of the flash memory cell is observed after erasing from the drain. Trapped holes in the oxide near the drain junction are found to be responsible for this degradation. Hole trapping in the oxide also causes another problem known as "gate disturb," which is the undesired increase in the threshold voltage of an erased cell during programming of the other cells on the same word line. Threshold-voltage shifts due to gate disturb are used to monitor the amount of trapped holes in the oxide after cell erasure. It is determined that the trapped holes are mainly externally injected from the junction depletion region rather than directly generated in the oxide by the Fowler–Nordheim (F–N) tunneling process.

FLASH memory [1]–[3] has recently emerged as an important nonvolatile memory which combines the advantages of EPROM density with EEPROM electrical erasability. Programming of the cell is achieved by hot-electron injection at the drain side, and erasure is usually accomplished by electron tunneling from the floating gate to either the drain [2] or the source [1], [3]. However, due to the presence of high voltage at the gated-diode junction during erasure, holes are inevitably generated by band-to-band tunneling [4] and a small amount of them are injected into the oxide after being accelerated in the depletion region. Hot-hole injection during erasure has been reported to cause variations in the erased threshold voltages of the cells in the memory array [1], and trapped holes in the oxide were shown to degrade the charge-retention characteristics of the memory cells [5]. However, no work has been reported on the effect of hole trapping on the programmability of the flash cell when erasing is done at the drain. In this work this effect is studied and the degradation in programmability is characterized. Since hole trapping in oxide is known to alter the tunneling characteristics of the oxide [6], [7], we have devised a method to compare hole trapping produced by Fowler–Nordheim (F–N) tunneling with that produced by hot-hole injection. Results clearly demonstrate that oxide hole trapping in flash structures is indeed attributable to the externally injected hot holes.

The flash cell used in this work has a structure very similar to that of a conventional stacked-gate EPROM cell. The channel length is about 1 μm long and the S/D arsenic diffusion is about 0.25 μm deep. The gate oxide used is less than 120 Å thick and the erasure mechanism is dominated by F–N tunneling [7]. In Fig. 1(a) three dc programming curves are presented for a fresh cell, for the cell electrically erased from the source, and for another cell electrically erased from the drain. It shows significant degradation in the programmability of the cell that has been erased from the drain side. Fig. 1(b) shows the programmed and erased threshold voltages as a function of the number of program/erase (P/E) cycles for a cell erased from the source and another erased from the drain. Fig. 1(b) clearly shows the programming threshold voltage is reduced after erasure from the drain, and as the cell is cycled the programming window continues to close. No degradation in the programmability is observed after erasure from the source. We believe that the degradation in programmability is caused by hole trapping in the oxide.

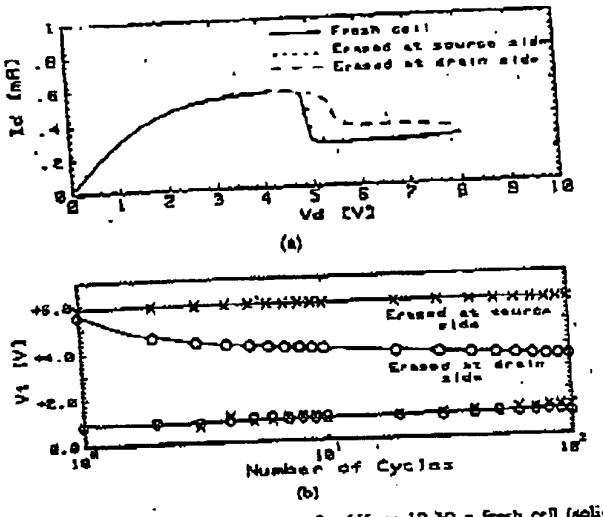


Fig. 1. (a) DC programming curves for (V_g = 12 V) a fresh cell (solid), electrically erased from the source side (dotted), and electrically erased from the drain side (dashed). (b) Programming/erase threshold voltage of the flash memory cell versus number of cycles, for drain-side and source-side erasure.

To demonstrate hole trapping in the oxide as a result of high-voltage erasure, poly gate transistors with similar gate oxide thickness and junction profile to the flash cell were used to monitor the hot-electron-generated substrate current and the gated-diode leakage current before and after the high-voltage stress. The stress was performed by applying a constant voltage of 11.5 V to the drain junction for 10 s while the gate and substrate were grounded with the source left floating. Fig. 2(a) shows the substrate current as a function of the gate voltage for V_D = 4 V, before and after the stress. The substrate current becomes lower after the stress due to a

Manuscript received October 21, 1988; revised December 19, 1988
The authors are with Advanced Micro Devices, Inc., Sunnyvale, CA 94088.
IEEE Log Number 8926657.

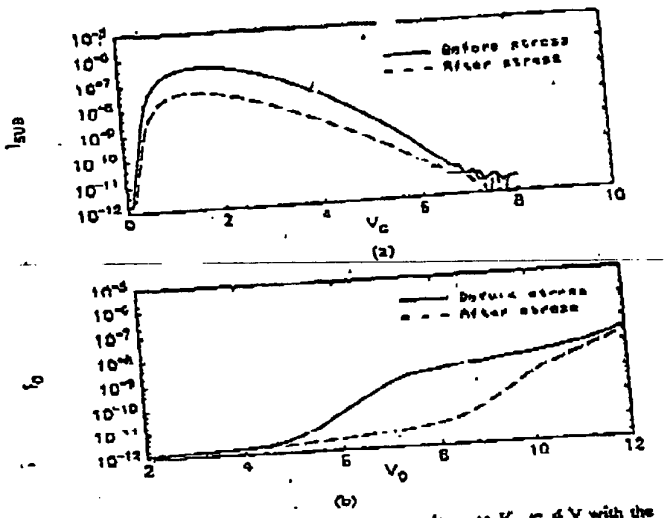


Fig. 2. (a) Substrate current versus the gate voltage at $V_D = 4$ V with the source grounded. (b) Drain leakage current versus drain voltage at $V_G = 0$ V with the source floating, measured before (solid) and after (dashed) high-voltage stress ($V_D = 11.5$ V for 10 s).

reduction in the channel field, indicating hole trapping in the oxide near the drain junction [8]. Fig. 2(b) shows the band-to-band tunneling current as a function of the drain voltage before and after stress. The drain leakage current versus V_D curve after the stress is shifted to a much higher drain voltage, also suggesting the fact that the surface field at the junction corner has been reduced due to hole trapping [4]. Hole trapping in the oxide near the drain has the effect of reducing the maximum channel electric field during programming, thereby decreasing channel hot-electron generation. This explains the degradation in programmability after drain-side erase.

By erasing from the source, programmability degradation is eliminated and, furthermore, the drain and source junctions can be independently optimized. The drain junction can be made shallow and abrupt to enhance the hot-electron effect for programming, and the source junction can be graded (for example, using a double-diffused junction) to reduce the junction field during erasing. A flash cell using this concept, which was first proposed by Kume *et al.* [1], is used in the following study to determine the origin of the trapped holes in the oxide during the erase cycle.

It is known that hole trapping inside the oxide reduces the barrier for electron tunneling [6]. This barrier lowering effect will lead to the so-called "gate disturb" problem for a memory array. Gate disturb refers to the undesired increase in the threshold voltage of the unselected "erased" cell during programming of the other cells on the same word line. During programming, a fraction of the word-line voltage will be coupled to the floating gate, and a high field (about 6–7 MV/cm) will appear across the thin gate oxide. As a result, electrons can tunnel to the floating gate through the thin oxide, causing the threshold voltage to increase. The gate disturb at a given field is proportional to the F-N tunneling current which is enhanced by the hole trapping in the oxide. Therefore gate disturb is used in this work as a monitor of the amount of trapped holes in the oxide due to erasure.

We believe that holes were introduced into the oxide through hot-hole injection during flash erasure. However, another possible mechanism is hole generation by impact ionization in the oxide during F-N tunneling itself [9], similar to that experienced in EEPROM erasure. The gate disturb test was used to compare positive charge trapping in the oxide using flash erasure with that using EEPROM-type erasure. For EEPROM-type erasure a negative voltage pulse (−16 V) is applied to the control gate, while the source junction is kept at a low positive voltage (2 V). The source voltage is low enough not to generate hot holes, while electron tunneling still occurs predominantly at the gate–source overlap region. On the other hand, the flash erasure is exercised by applying a high positive voltage pulse (11 V) to the source with the gate grounded and the drain floating. Fig. 3 shows the threshold voltage of the flash cell versus the erase time using the two different erase conditions mentioned above. For both erasures, the erasing speed is controlled by F-N tunneling. The voltages were chosen such that the oxide field during the EEPROM-type erasure is slightly larger than that for the flash erasure. This is done to ensure that the F-N tunneling-induced hole generation in the oxide for the EEPROM-type erasure is no less than that in the flash erasure.

Fig. 4 compares the gate disturb after EEPROM and flash erasures. The cell was first alternately programmed and erased to V_t's of 6 and 1 V, respectively, for 20 cycles in order to saturate the hole trapping in the oxide. Then the threshold voltage was measured as a function of gate disturb time. During the gate disturb, the gate of the erased cell was biased at 12 V while the other terminals were at ground. As shown in the figure, no V_t shift is observed for the cell erased under EEPROM condition. This suggests that the holes that are

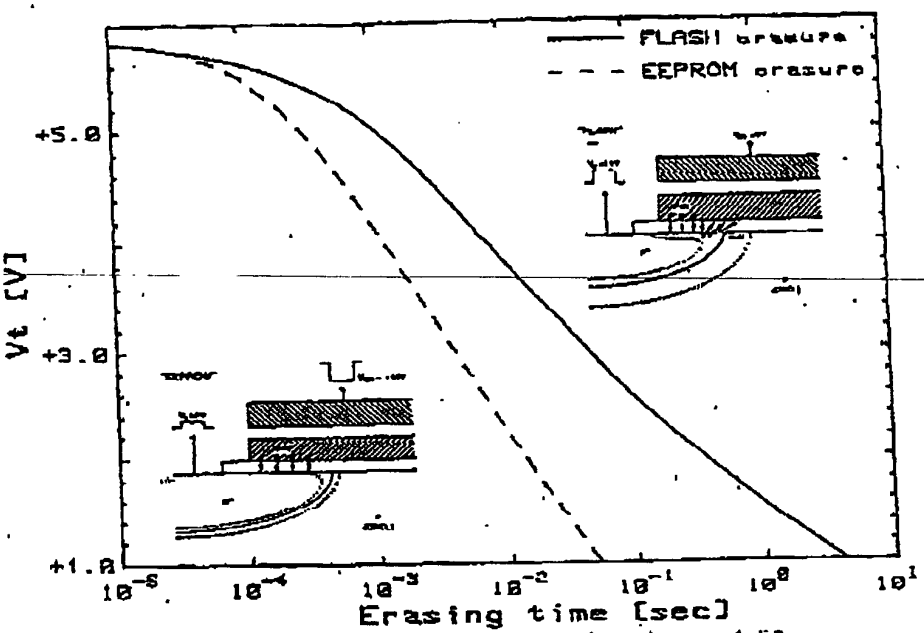


Fig. 3. Threshold voltage versus erasing time during flash erasure (solid) and EEPROM-type erasure (dashed). The faster erasure time of the EEPROM-type erasure is due to the higher applied field across the oxide. The insets are schematic representations of the two erase conditions.

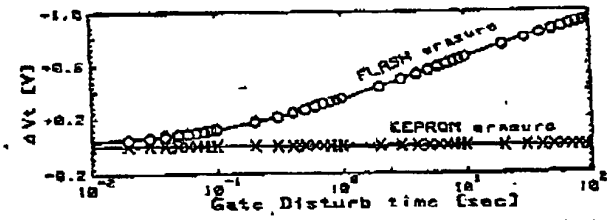


Fig. 4. Threshold-voltage shifts ($\Delta V_t = V_t - V_t$(before disturb)) during gate disturb after the cells having been cycled 20 times, using flash (○) and EEPROM (×) erasure. The cells were erased to a V_t of 1 V before gate disturb measurement.

generated and trapped in the oxide by the F–N tunneling electrons are insignificant in contributing to gate disturb. However, the gate disturb after the flash erasure is significant. These data strongly support a model of external hot-hole injection and hole trapping in the oxide during the flash erasure.

In summary, we have demonstrated that the hot-electron programming efficiency of the flash cell is degraded after erasure from the drain. Degradation in programmability has been shown to be caused by trapped holes in the gate oxide at the drain junction. By comparing the flash erasure to EEPROM-type erasure, it has been determined that these trapped holes are externally injected from the junction depletion region. Furthermore, the trapped holes in the gate oxide will lead to gate disturb. Therefore, in a properly designed flash structure, it is essential that hot-hole injection is minimized.

References

[1] H. Kume *et al.*, "A flash-erase EEPROM cell with an asymmetric source and drain structure," in *IEDM Tech. Dig.*, 1987, pp. 560–563.

[2] G. Samachisa *et al.*, "A 128K flash EEPROM using double-polysilicon technology," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 676–683, Oct. 1987.

[3] S. Mukherjee, T. Chang, R. Pang, M. Knecht, and D. Hu, "A single transistor EEPROM cell and its implementation in a 512K CMOS EEPROM," in *IEDM Tech. Dig.*, 1985, pp. 616–619.

[4] C. Chang and J. Lien, "Corner-field induced drain leakage in thin oxide MOSFET's," in *IEDM Tech. Dig.*, 1987, pp. 714–717.

[5] G. Verma and N. Mielke, "Reliability performance of ETOX based flash memories," in *26th Proc. IEEE Reliability Phys. Symp.*, Apr. 1988, pp. 158–166.

[6] I. C. Chen, S. Holland, and C. Hu, "Electrical breakdown of thin gate and tunneling oxides," *IEEE Trans. Electron Devices*, vol. ED-32, no. 2, pp. 413–422, 1985.

[7] C. Chang, S. Haddad, B. Swaminathan, and J. Lien, "Drain avalanche and hole-trapping induced gate leakage in thin-oxide MOS devices," *IEEE Electron Device Lett.*, vol. 9, no. 11, pp. 588–590, 1988.

[8] Y. Nissan-Cohen, G. Frantz, and R. Kwasnick, "Measurement and analysis of hot-carrier-stress effect on NMOSFET's using substrate current characterization," *IEEE Electron Device Lett.*, vol. EDL-8, pp. 451–453, 1987.

[9] I. C. Chen, S. Holland, and C. Hu, "Hole trapping and breakdown in thin SiO_2," *IEEE Electron Device Lett.*, vol. EDL-7, no. 3, pp. 164–166, 1986.